FIG. 1

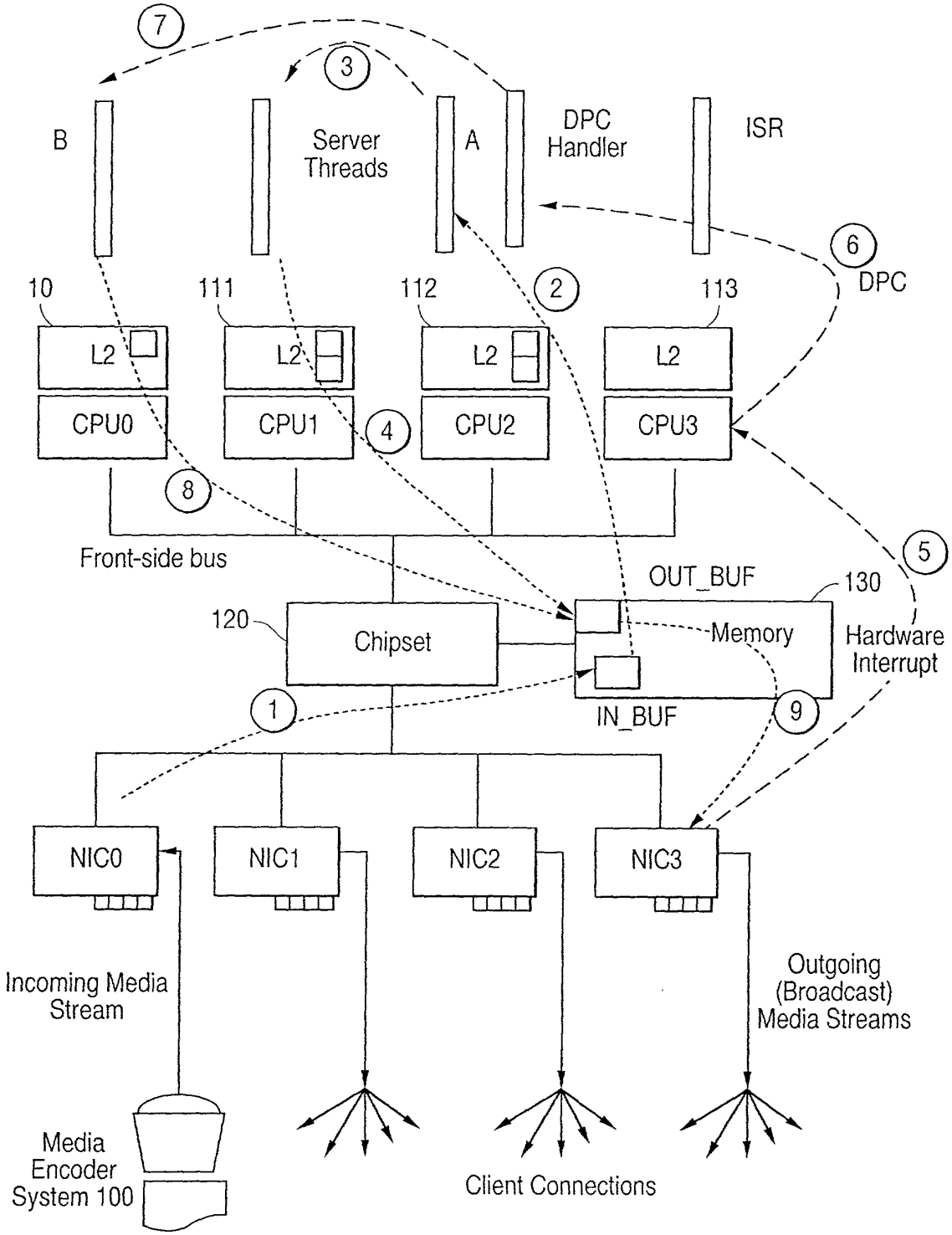
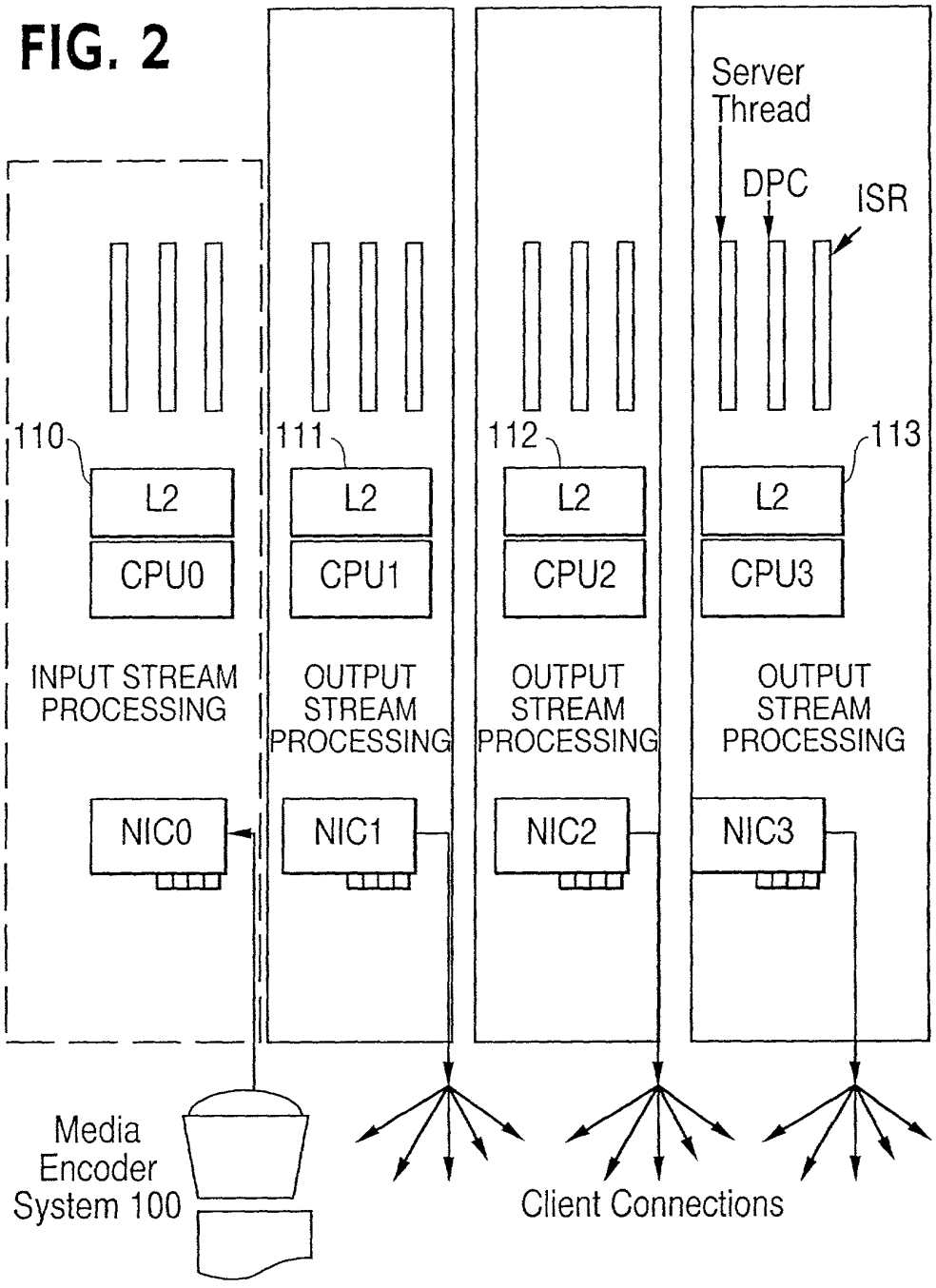

7
3
B
Server Threads
A
DPC Handler
ISR
6
DPC
10
111
112
2
113
L2
L2
L2
L2
CPU0
CPU1
4
CPU2
CPU3
8
Front-side bus
5
OUT_BUF
130
120
Chipset
Memory
Hardware Interrupt
1
IN_BUF
9
NIC0
NIC1
NIC2
NIC3
Incoming Media Stream
Outgoing (Broadcast) Media Streams
Media Encoder System 100
Client Connections

FIG. 2


Server Thread
DPC
ISR
110
111
112
113
L2
L2
L2
L2
CPU0
CPU1
CPU2
CPU3
INPUT STREAM PROCESSING
OUTPUT STREAM PROCESSING
OUTPUT STREAM PROCESSING
OUTPUT STREAM PROCESSING
NIC0
NIC1
NIC2
NIC3
Media Encoder System 100
Client Connections

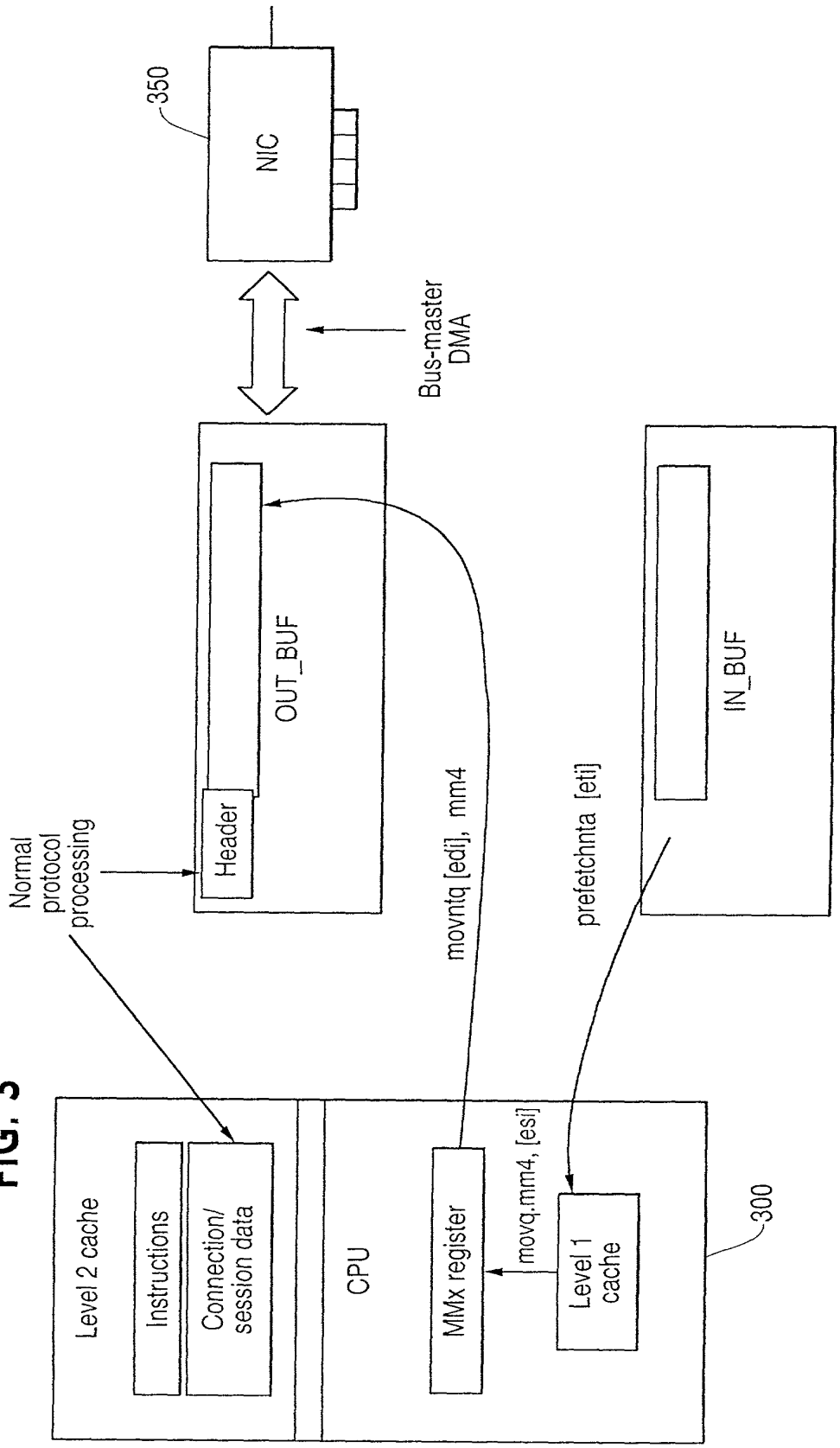
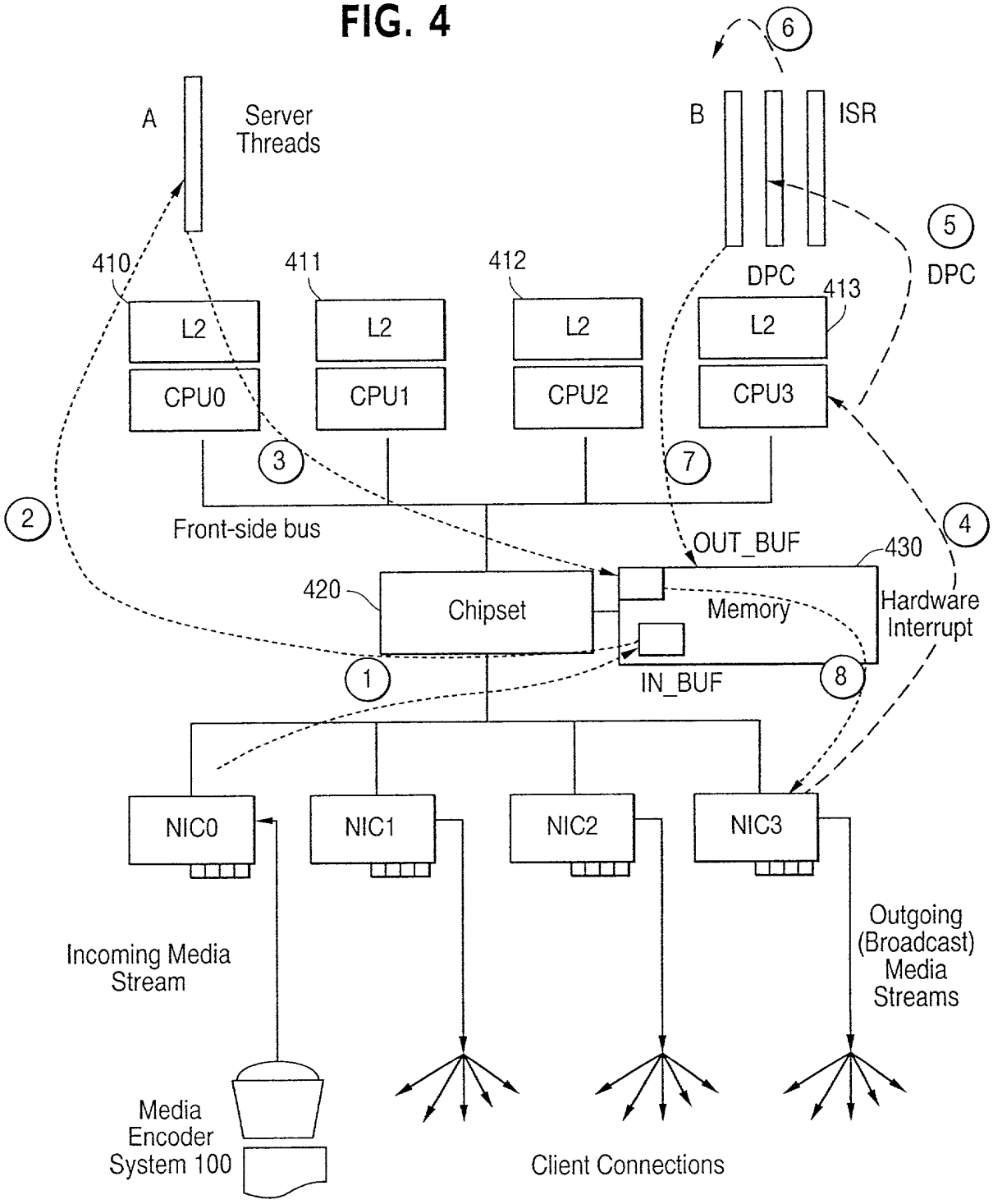

350
NIC
Bus-master DMA
OUT_BUF
Header
IN_BUF
Normal protocol processing
movntq [edi], mm4
prefetchnta [eti]
Level 2 cache
Instructions
Connection/ session data
CPU
MMx register
movq.mm4, [esi]
Level 1 cache
300

FIG. 3

FIG. 4


A
Server Threads
B
ISR
6
5
DPC
DPC
410
411
412
413
L2
L2
L2
L2
CPU0
CPU1
CPU2
CPU3
3
7
2
Front-side bus
OUT_BUF
430
4
420
Chipset
Memory
Hardware Interrupt
1
IN_BUF
8
NIC0
NIC1
NIC2
NIC3
Incoming Media Stream
Outgoing (Broadcast) Media Streams
Media Encoder System 100
Client Connections